REMARKS

Pending Claims

Claims 12-26 are currently pending. Claims 1-11 were previously canceled. Claims 12-18 and 24-26 are currently amended to improve clarity. No new matter is added.

Rejections Under 35 U.S.C. § 103

Claims 12-16 and 24-26 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of what the Examiner has identified as the Applicant Admitted Prior Art ("AAPA") in view of Miyashita et al. (USP 5,610,954). In addition, claims 19-22 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of the AAPA in view of Miyashita et al. further in view of Yonekura et al. (USP 5,761,617). Further, claims 17-18 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of the AAPA in view of Miyashita et al. further in view of Anumula et al. (USP 6,566,967). Finally, claim 23 stands rejected under 35 U.S.C. § 103(a) as being obvious over the combination of the AAPA, Miyashita et al., Anumula et al. and further in view of Yonekura et al. However, in view of the amendments to and the arguments presented herein, Applicant respectfully submits that the rejections have been traversed and request that the rejections be reconsidered and withdrawn.

The combinations of references cited by the Examiner fail to render the claims obvious because none of the combinations of references teaches or suggests all of the elements of the claimed combinations. Among other distinctions, neither the AAPA nor Miyashita et al. teaches or suggests a clock and data recovery circuit which includes: "a phase detector circuit for detecting the phase difference between an output data signal, discriminated and output by said discriminator circuit, and said input data signal" (claim 12); "a second phase detector circuit for detecting the phase difference between an output data signal, discriminated and output by said discriminator circuit, and said received data signal" (claim 13); or "a second phase detector circuit for detecting the phase difference between an output data signal discriminated and output by said discriminator circuit and said received data signal" (claim 15).

In Figure 11 of the present application (the AAPA), the discriminator 904 emits the Data Out signal, which is not fed back into any portion of the circuit. In Figure 7 of Miyashita et al.,

the Examiner argues that elements 21A and 21B together form the discriminator circuit, the output of which is designated RDATA. The Examiner also argues that element 22A, whose inputs are DATA IN and QA, performs phase comparison between the input data signal and the discriminator output. However, the output of what the Examiner has designated as the discriminator, namely RDATA, is not fed back to the phase comparison element 22A. Thus, neither the AAPA nor Miyashita et al., alone or in combination, teaches or suggests a clock and data recovery circuit having a phase detector circuit which detects the phase difference between the discriminated output signal and the input data signal, nor do any of the other cited references supply the deficiencies.

The remaining claims are allowable because each depends from one of the allowable independent claims 12, 13, and 15, and because each dependent claim recites additional patentable subject matter.

CONCLUSION

In view of the remarks and amendments presented herein, reconsideration and withdrawal of the pending rejections and allowance of the claims are respectfully requested. The Examiner is strongly encouraged to contact the undersigned at the phone number below should any issues remain with respect to the application.

Respectfully submitted,

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